PICTURE SYSTEM 2
Maintenance Manual
Volume 2
Line Generator and Character Generator

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5.0 THE CHARACTER GENERATOR

5.1 Character Generation

The PS-2 and MPS Character Generators are functionally identical. They contain a PROM character memory programmed to interpret the 128 ASCII character set and generate the strokes or vectors for the 95 displayable ASCII characters. In addition to the pre-programmed PROM the Character Generator contains a 1024 word by 12-bit RAM which the user can employ to generate the strokes for character sets of his own design. A detailed description of the 128 ASCII character and control codes which the pre-programmed PROM interprets is presented in sections 2.4.4.1, Standard Character Sizes and Definitions, of the PS-2 and MPS Reference Manual. The scale or size of the displayed characters, their orientation and slant are obtained by multiplying the basic stroke data by "coefficients". The character multiplier of the Character Generator contains PROM storage for 16 sets of multiplying coefficients and a RAM into which the user may program 32 sets of coefficients.

The character memory is programmed with sequences of instructions from a set of five drawing and control instructions. One of these instructions is employed to define the individual strokes of each character which the Character Generator is capable of displaying. This instruction is the

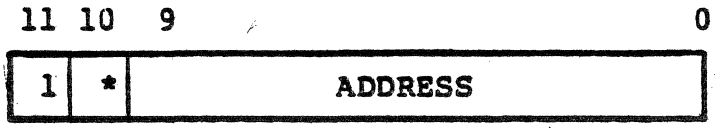
CHDRAW/CHMOVE instruction. A second instruction, RMOVE, is used to define the moves between successive characters and to indicate that the last stroke of the set of strokes defining the character has occurred.

A third instruction, JMS, the Ju Mp Subroutine, is employed to point to the first CHDRAW/CHMOVE instruction of the sequence of stroke defining instructions.

The character memory is addressed by the four character codes (ASCII codes) of the Line Generator CHARACTER COMMAND words. (See Table 2-2: REFRESH CONTROL and CHARACTER COMMAND Bit-Bus Assignment - page 2-12). The instruction existing at this character memory location is a JMS which points to the first CHDRAW/CHMOVE instruction of the sequence defining the character strokes. Hence the first 128 locations of the character memory contain JMS instructions whose address fields contain the starting locations of the character stoke sequence or sequences of control instructions for those ASCII codes that do not display characters. The sequence of stroke instructions for a character is terminated by an RMOVE.

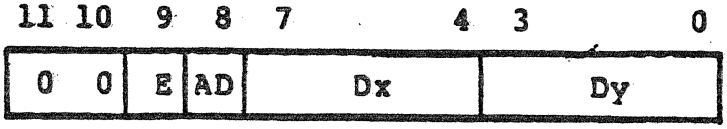
The format of the JMS, CHDRAW/CHMOVE and the REMOVE instructions are:

JMS



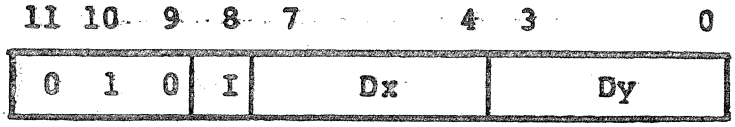
*=0: ADDRESS is within PROM
*=1: ADDRESS is within RAM

RMOVE



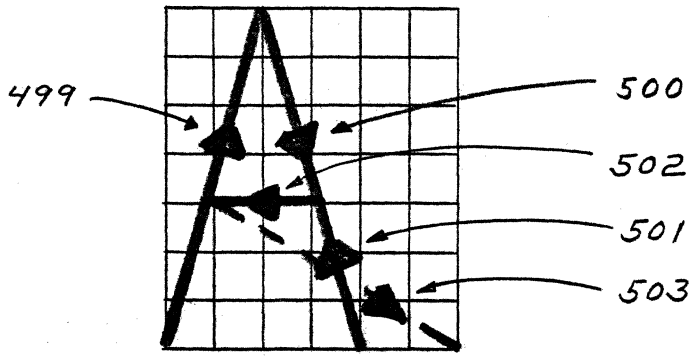
E=0: Not End
E=1: End
AD=0: Do Not Add Displacement to Dx and Dy
AD=1: Add Displacement to Dx and Dy

CHDRAW/CHMOVE



I=0: CHMOVE (Do Not Intensify)
I=1: CHDRAW (Intensify)

The use of these instructions to generate the strokes for the capital A character is shown in Figure 5.1. The input code from the CHARACTER COMMAND WORD is the ASCII code (101_8) for a capital A which addresses character memory location 65. Location 65 contains a JMS whose bit 10 causes a jump to PROM location given by address bits 9-Ø; location 499. Character



INPUT ASCII Code = 101_8 = 0 0 1 0 0 0 0 0 1

LOCATION 65

CHARACTER MEMORY LOCATION	MEMORY CONTENTS OCTAL	INSTRUCTION	INSTRUCTION	CONTENT	BINARY
65	111703	JMS	1 0 0 1	1 1 1 1 499	0 0 1 1
499	050207	CHDRAW	0 1 0 1 I = 1	0 0 1 0 ΔX = 2	0 1 1 1 ΔY = 7
500	050211	CHDRAW	0 1 0 1 I = 1	0 0 1 0 ΔX = 2	1 0 0 1 ΔY = -7
501	041703	CHMOVE	0 1 0 0 I = 0	1 1 1 1 ΔX = -1	0 0 1 1 ΔY = 3
502	051600	CHDRAW	0 1 0 1 I = 1	1 1 1 0 ΔX = -2	0 0 0 0 ΔY = 0
503	020615	RMOVE	0 0 1 1 E = 1 AD = 1	0 1 1 0 ΔX = 6	1 1 0 1 ΔY = -3

FIGURE 5.1
CHARACTER MEMORY - TYPICAL STROKE SEQUENCE

memory location 499 contains a CHDRAW instruction whose binary code is shown in the rightmost column. Notice that the intensity bit, bit-8, is a 1 indicating a draw of $\Delta X = 2$ and $\Delta Y = 7$. This stroke is "mapped" on the character matrix above as 499. The "map" of the remaining CHDRAW and CHMOVE instruction strokes denoted by their character memory locations 500, 501 and 502. The final instruction, location 503, is an RMOVE. Notice that $\Delta X = 6$ and $\Delta Y = -3$ are a move to the lower left starting point of a possible next character. The end of this sequence of strokes is indicated by bit 9, the end-bit, of RMOVE being a one. The basic stroke data, ΔX and ΔY, are the processed further by the character multiplier to produce characters of various sizes, orientations, slant, etc. This processing consists of multiplying the ΔX and ΔY data by a four by four "coefficient matrix" whose elements are A, B, C, and D.

$$[\Delta X', \Delta Y'] = [\Delta X, \Delta Y] \begin{bmatrix} A & C \\ B & D \end{bmatrix}$$

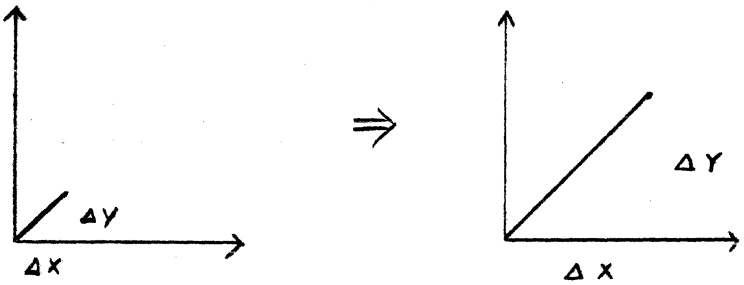
Figure 5.2 shows two examples of how the basic stroke data may be modified by this process. Figure 5.2 (a) illustrates a character size or scale change and 5.2 (b) the rotation of the strokes required to display a vertically written character.

$$[\Delta X', \Delta Y'] = [\Delta X, \Delta Y] \begin{bmatrix} A & C \\ B & D \end{bmatrix}$$

(a) SCALE OR SIZE CHANGE by 3

$A = 3$
$B = 0$
$C = 0$
$D = 3$

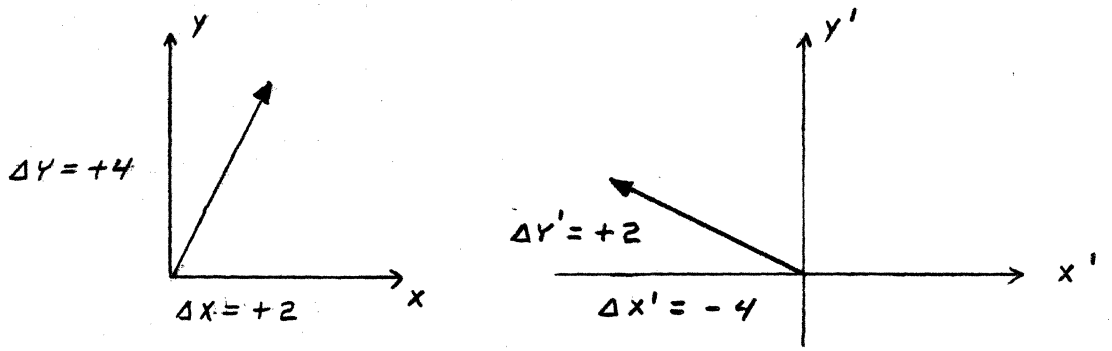
$$[\Delta X', \Delta Y'] = [\Delta X, \Delta Y] \begin{bmatrix} 3 & 0 \\ 0 & 3 \end{bmatrix} = [3\Delta X, 3\Delta Y]$$



(b) TO GENERATE VERTICAL CHARACTERS

$A = 0$
$B = -1$
$C = 1$
$D = 0$

$$[\Delta X', \Delta Y'] = [\Delta X, \Delta Y] \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} = [-\Delta Y, \Delta X]$$



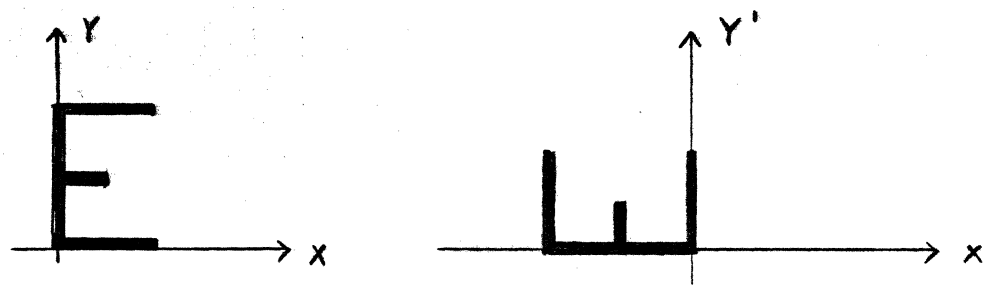
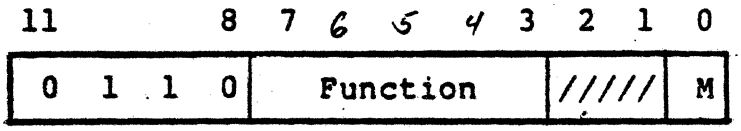


FIGURE 5.2
CHARACTER MULTIPLIER EXAMPLES

After processing to obtain the desired scale, orientation, etc., the modified stroke data, $\Delta X'$ and $\Delta Y'$, are output onto the XCBUS and YCBUS and sent to the 195217, X-Y Adder-Shifter cards of the Line Generator. They are processed by the Line Generator as relative vector data.

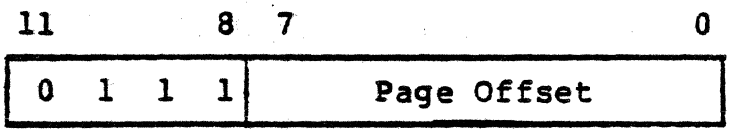
Three of the five instructions that are used in the internal programming of the character memory were described above. The remaining two instructions are the CONTROL instruction and the JMP, Ju Mp Page, instruction. The JMP is used to transfer the control of the character generation instructions to the location offset specified within the current page. This instruction is necessary as the character memory is considered to be four 256 word pages (0-255, 256-511, 512-767, 768-1023) and it is not possible to cross page boundries using the JMP instruction. The CONTROL command instruction is used to perform the functions required in character generation which are other than those of generating the actual strokes. Typical operations that must be performed are carriage return, save a character position as left and top margin and save a position as the carriage return position. The format of CONTROL and JMP are:

CONTROL



Function= Function to be performed (see below)
M= Modifier - Function dependent (see below)

JMP



A description of all five character generation instructions is given in the PS-2 and MPS Reference Manuals, section 2.4.4.3 character memory.

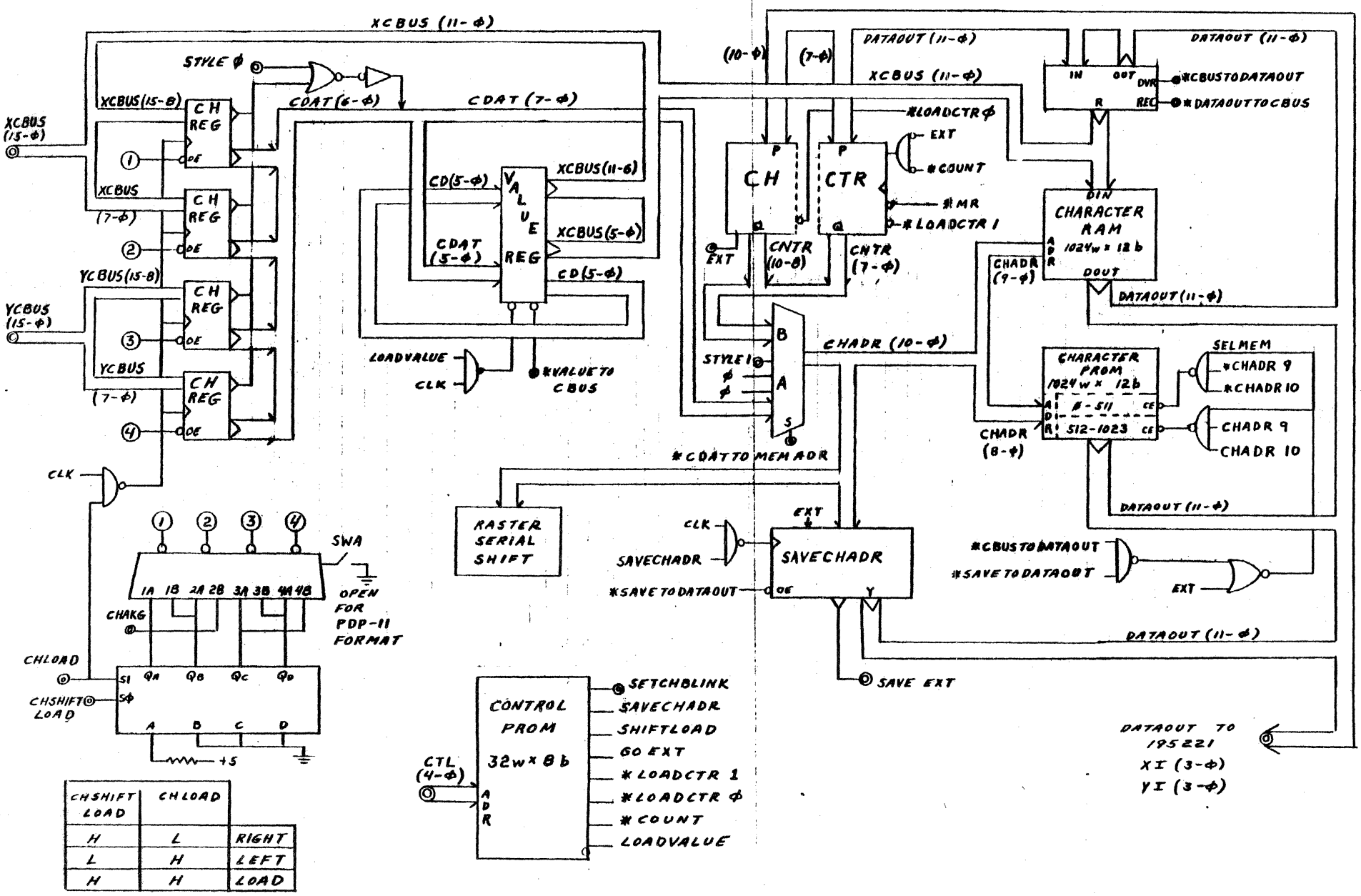
5.2 Character Memory - Multiplier Implementation

The Character Generator is implemented in a three card set. It is a true hardware option in the sense that the three cards can be physically removed from the PS-2 or MPS back-panel without affecting the operation of the remainder of the system. These three cards are:

195221 - Character Multiplier
195222 - Character Memory
195223 - Character Control

The Character Memory, Character Multiplier and their data buss structures are shown by the block diagrams of Figure 5.3 - Character Memory 195222 card and 5.4 - Character Multiplier 195221 card.

The character code input registers, CH, are shown at the left of Figure 5.3. The four, seven bit, character codes of the CHARACTER COMMAND word from the input FIFO are clocked into CH REG when CHLOAD is high. These four codes are distributed on the XCBUS and YCBUS as shown in Table 2-2, page 2-12, for the CHARACTER COMMAND. Thus the CH registers, from top to bottom, contain the character codes Ø-3. The destinations of these character codes, CDAT (7-Ø),



CHSHIFT LOAD	CHLOAD	
H	L	RIGHT
L	H	LEFT
H	H	LOAD

FIGURE 5.3

BLOCK DIAGRAM - CHARACTER MEMORY 195222 CARD

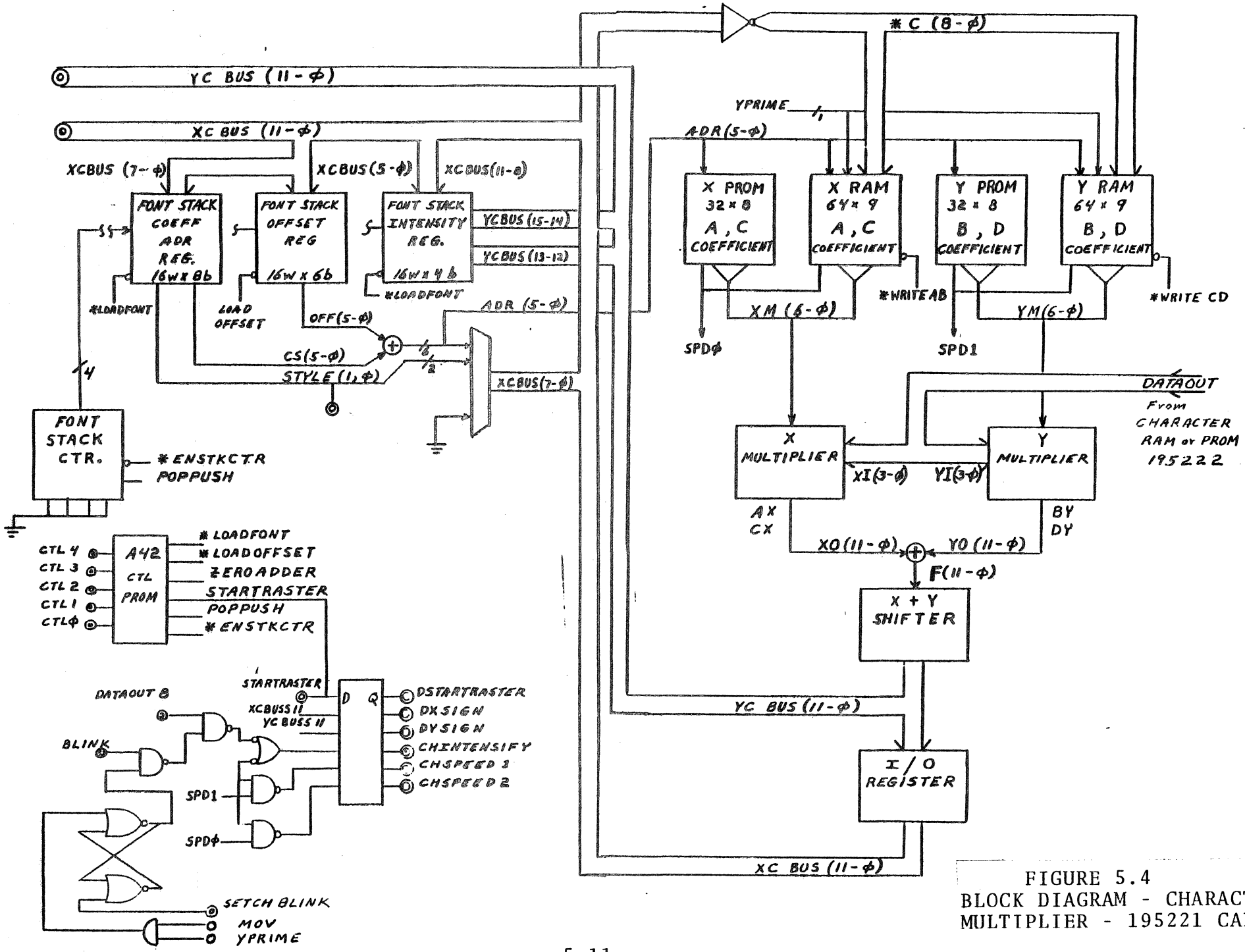


FIGURE 5.4
BLOCK DIAGRAM - CHARACTER MULTIPLIER - 195221 CAPD

are the CHARACTER RAM and CHARACTER PROM address inputs. The codes are sequentially selected onto the tri-state CDAT (7-Ø) bus by the select control shown at the lower left. This control generates the four CH register output enables 1, 2, 3 and 4 by means of a four bit shift register. When CHLOAD and CHSIFT are both high the shift register is loaded with a H in the least bit (Q_A) and lows in Q_B thru Q_D. If CHLOAD goes low this least H is shifted to Q_B, Q_C and Q_D on successive clock inputs. Note that a low CHLOAD prohibits new codes from being input to the CH register by inhibiting their clock inputs.

The 2 to 1 multiplexer is normally operated with switch SWA closed and the CH register outputs are selected onto CDAT in the top to bottom sequence. If SWA is open the sequence becomes XCBUS (7-Ø), XCBUS (15-8), YCBUS (7-Ø) and YCBUS (15-8) as the B inputs to the multiplex are applied to the CH output enables. The switch makes it possible to use the DEC, PDP-11 character code format. Note that bit 7 of CHDAT is generated by ORing STYLEØ with bit seven of the CHARACTER CODE as shown above the CH REGISTER.

The Character Memory Address Selector, shown in the center of the black diagram selects either CDAT (7-Ø), two zeros and STYLE1 or the eleven bits of the character counter, CHCTR, as the address input, CHADR (10-Ø), to the CHARACTER

RAM or CHARACTER PROM. The eight bits of CDAT (7-Ø), the two zeros and the STYLE1 bit are selected when a new character code is input. These bits are the RAM or PROM address of the JMS instruction that points to the RAM or PROM location of the first of the sequence of stroke instructions that define the character. The address pointed to by the JMS is output by the RAM or PROM, DATAOUT (11-Ø), and loaded into the character counter, CHCTR, whose output is connected to the "B" input of the CH MEM Address Selector. The "B" input is selected by the Address Selector and the sequential stroke addresses presented to the RAM or ROM are generated by incrementing CHCTR. The four bits of ΔX and ΔY output by the CHDRAW/CHMOVE instructions are sent to the Character Multiplier via the DATAOUT bus as shown at the lower right; XI (3-Ø) and YI (3-Ø).

The SAVECHADR register shown below the Character Memory Address Selector provides a means of saving a character memory address and outputting it on the DATAOUT bus. This capability is required to store the character memory return address for the JMS insturction.

As mentioned above the user can program the CHARACTER RAM to provide many capabilities which are not available with the character PROM. The RAM is also programmed with the five in-

structions described above which are 12 bit words. These 12 bit words are constructed from the 8 bit character code words of the CHARACTER COMMAND words. The VALUE REGISTER shown in the upper left is used to assemble 12 bit words for the RAM from 8 bit inputs. The least 6 bits of an 8 bit CH REG output, CDAT (5-Ø), are input to the "lower half" of the VALUE REG, the output CD (5-Ø) are fed back to the upper half of the VALUE REG and six from a second CH REG are loaded into the lower half of the VALUE REG. The 12 bit output of the VALUE REG are loaded into the RAM via the XCBUS lines 11-Ø. A description of the user available programming features of the CHARACTER RAM is provided in section 2.4.4.5 of the PS-2 and MPS Reference Manual.

The RASTER SERIAL SHIFT register shown below the VALUE REG implements a function that is not used in the Character Generator.

The 12 bit transceiver shown above the CHARACTER RAM, upper right, allows the Character Memory outputs, DATAOUT, to be put onto the XCBUS and XCBUS data to be directed onto the DATAOUT bus.

The 32 word by 8 bit CONTROL PROM converts the control signals CTL (4-Ø) from the CHARACTER CONTROL DO IT REGISTER of

the 195223 card into the control signals shown.

Figure 5.4 is a Block Diagram of the Character Multiplier (195221) card. The ΔX and ΔY multiplication by the A, B, C and D coefficients is shown on the right. A and C coefficients are stored in the 32 word by 8 bit X PROM and the B and D coefficients in the 32 word by 8 bit Y PROM. The X RAM and Y RAM can be programmed with A, B, C and D coefficients that are defined by the user. The multiplications A.ΔX and C.ΔX are performed by the X Multiplier and B.ΔY and D.ΔY by the Y Multiplier. The XI (3-Ø) and YI (3-Ø) inputs are received from the Character Memory card on the DATAOUT bus. The multiplication process is performed in two steps. Step one generates A.ΔX and B.ΔY, adds them, shifts appropriately and stores the result in the I/O REGISTER. Step two generates C.ΔX and D.ΔY, adds them and shifts appropiately. This result and the result in the I/O register are sent to the Line Generator (195217 Adder- Shifter cards) over the YCBUS and XCBUS at the same time.

The eighteen bits which describe the character intensity and style and the coefficient address and coefficient offset are stored in the 16 word FONT STACK register shown at the upper left of the diagram. The 8 bit FONT STACK - COEFF ADR REG contains the two style bits and a six bit coefficient address.

The two style bits provide four selectable character styles, two in the CHARACTER PROM and two in the RAM. The selectable styles in the PROM are "regular" and "fast". Style bit 1 selects PROM if Ø and RAM if a 1. Style bit Ø along with the eight bits of the actual input character code make up the Character Memory Address (CHADR) selecting the beginning location of the character stroke sequence. The six bit coefficient address, CS (5-Ø) specifies 32 coefficient locations in the coefficient PROMS or 64 locations in the coefficient RAMS. The FONT STACK - OFFSET REGISTER contains a six bit coefficient offset, OFF (5-Ø), which may be added or subtracted from the coefficient address to allow indexing within a basic set of coefficients. The final address, ADR (5-Ø), addresses the A, B, C and D coeffiecient PROM's and RAMS. The FONT STACK - INTENSITY REGISTER contains 16 words of 4 bits of intensity which make it possible to specify character intensity independent of the MOVE or DRAW commands to the Line Generator. The CHARI bit of the Line Generator STATUS command word, see Table 2-2, if a one specifies that character intensity is to be taken from the FONT STACK - INTENSITY REGISTER.

The A42 CONTROL PROM at the lower left converts the control signals CTL (4-Ø) from the CHARACTER CONTROL - DO IT REGISTER of the 195223 card into the control signals shown.

5.3 Other Character Generator Logic

In addition to the three main cards of the Character Generator other cards in the Line Generator contain logic and memory necessary to the operation of the Character Generator.

The lower six registers, 2-6, of the X and Y Register Files on the 195217 X-Y Adder Shifter cards are used to store X,Y position data used by the Character Generator instructions. The assignment of these register file locations is shown on sheet 1 of the Arithmetic Control state diagram, 195216-950. These register file assignments are:

2 - XYSAVE
3 - XYHOME
4 - DXYDISPL
5 - DXYSUBDIPL
6 - XYSUB
7 - LIMIT

LIMIT is used as a temporary store for current XY position in performing carriage return, tab, linefeed and return to HOME. XYHOME saves a character position as left top margin, the HOME position. XYSAVE is used to store the carriage return position. XYSUB, DXYDISPL and DXYSUBDIPL are used in the character move plus displacement operation. This operation uses the Character Memory instruction RMOVE to cause the

current character position to be updated to the current position plus the ΔX and ΔY values specified by RMOVE. The specific Line Generator operations that employ these registers are the Character Generator state sequences of the Line Generator Arithmetic Controller; RESET, CHMOV + DISPLACEMENT, TESTLIMIT, SAVEHOME, CARRET, HOME, SAVE CARRET POSITION, and LIMITTOXY. These sequences are described in detail in Figure 3.6 of section 3.3 the Arithmetic Control State Machine (195216) of this manual.

Recall from the discussion above, section 3.1, the Four State Machine Controllers and section 3.2, the Input Control State Machine that when a CHARACTER COMMAND WORD is encountered by Input Controller it goes to state 20 (24), CHARACTER. The control bits passed onto the Arithmetic Controller will now come from the Character Control card, 195223, instead of the Line Generator Input Control card. (Refer to Figure 3.1 The Line Generator-Character Generator Controllers). The logic that implements this operation is shown in Figure 5.5 Line Generator-Character Generator Control Interface. This diagram is extracted from the logic on sheets 1, 3 and 4 of the 195218-600 Line Generator Input Control Logic. The sequence of events that occur when a CHARACTER COMMAND WORD is received is as follows:

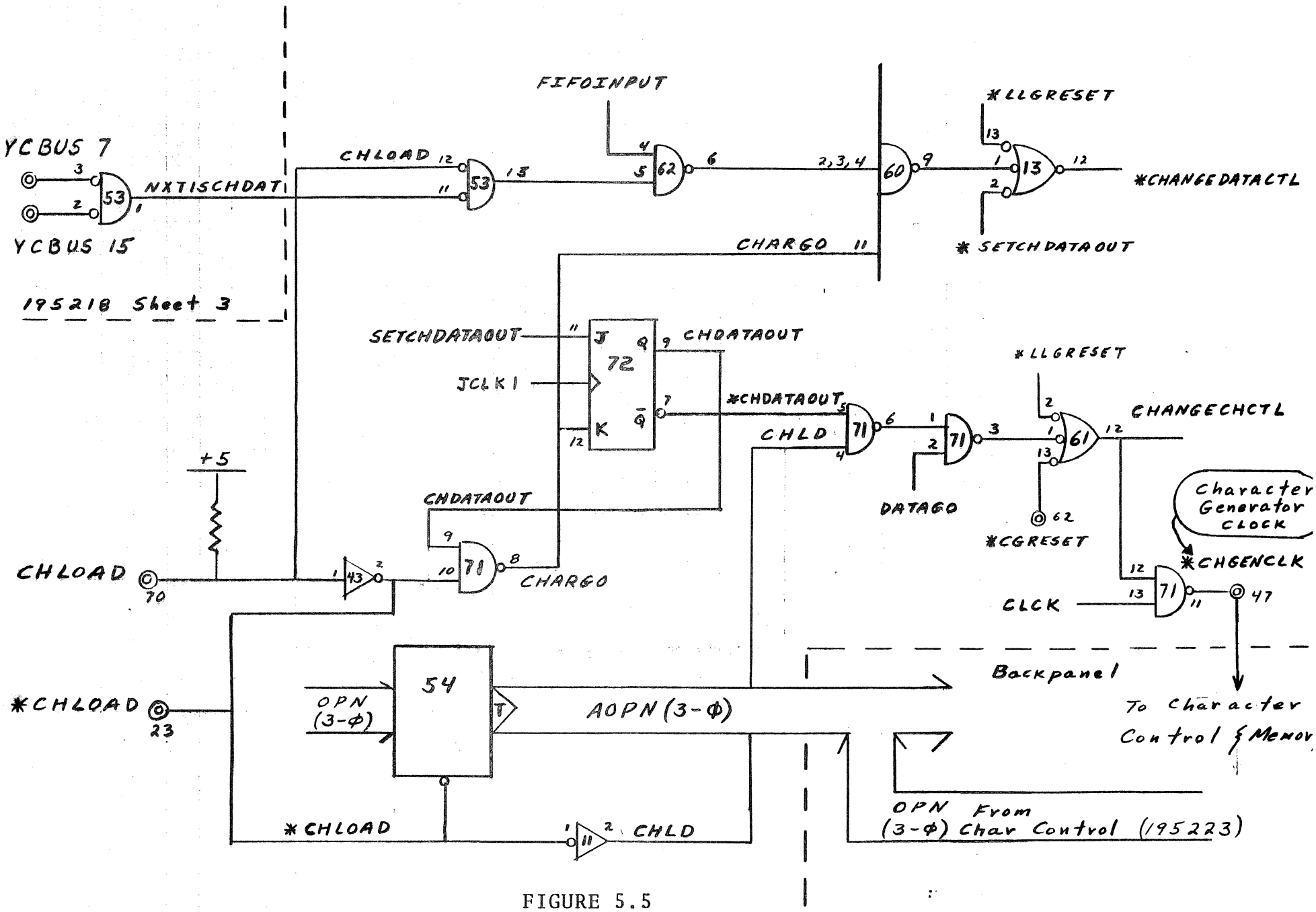


FIGURE 5.5

LINE GENERATOR - CHARACTER GENERATOR CONTROL INTERFACE

a) The Input Controller goes to state 20, 24 CHARACTER which generates SETCHDATAOUT.

b) On the next clock the CHDATAOUT flip-flop is set thus *CHDATAOUT goes low making 71.6 (71.1) high.

c) When DATAGO, which indicates that the Arithmetic Controller is ready to take in new control data, goes high 71.3 (61.1) go low, CHANGECHCTL goes high and the clock, *CHGENCLK, is gated out to the Character Generator Control card (195223) and Memory card (195222).

d) This clock strokes control data from the Character Generator control PROM into the DO IT Register.

e) One of those Character Generator control signals is CHLOAD which goes low. CHLOAD is used in the Character Generator to enable the OPN (3-Ø) code on to the AOPN (3-Ø) bus and on the Input Control card *CHLOAD disables the OPN (3-Ø) code of the Input Controller from the AOPN (3-Ø) bus. (Refer to the bus interface IC 54 at the bottom of Figure 5.5).

f) When CHLOAD goes low, CHARGO goes low and on the next clock the CHDATAOUT flip-flop is reset, *CH-DATAOUT goes high. As long as CHLOAD remains low CHLD remains low keeping 71.6 (71.1) high. Each time the Arithmetic Controller completes a path through one of its control sequences DATAGO will return high and *CHGENCLK will be enabled to the Character Generator.

The logic shown at the top of Figure 5.5 controls the generation of *CHANGEDATACTL, which controls sequencing through the states of the Input Controller during Character Generation. When CHDATAOUT is reset CHARGO goes high and remains high until a new CHARACTER COMMAND WORD is input and state 20 (24) is entered causing SETCHDATAOUT to go high and CHDATAOUT to be reset. Notice that *SETCHDATAOUT causes a *CHANGEDATACTL which returns the Input Controller to the RESET state where it is ready to accept a new input code from the FIFO. Thus during Character Generation FIFOINPUT is high but the input to gate 60, pins 2, 3 and 4, will remain low until CHLOAD or NXTISCHDAT or both go high. Thus the signal NXTISCHDAT keeps the Input Controller in State 20 (24) during the input of strings of characters.